# Experimental Results and Die Area Efficient Self-Shielded On-Chip Vertical Solenoid Inductors for Multi-GHz CMOS RFIC

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***Abstract* — On-chip circular vertical solenoid inductors have been designed and fabricated using standard 6-metal layer CMOS process. Compared to the 4.1nH circular planar spiral inductor on the same chip, the 4.8nH solenoid inductor gives about 20% increase in maximum quality-factor (QF) and 50% increase in self-resonant frequency (SRF), but only occupies 20% of the area. The inductor impedance can be modeled by a simple RLC circuit valid beyond 20GHz.**

## I. Introduction

Significant efforts have been done by researchers to improve the QF and SRF of CMOS on-chip inductor for radio-frequency (RF) circuit applications[1][2]. In this work, however, we aim at reducing the area occupied by the inductor which dominates the chip size, while further improving the QF and SRF. By taking the advantage of multi-metal layer provided by the modern digital CMOS process, the inductor size can be substantially reduced using solenoid structure. The inductor is self-shielded electrically from the lossy substrate and experimental results indicate that poly patterned-ground-shield (PGS), while useful in planar spiral inductor, is not needed for solenoid inductor for better performance. The compact structure and self-shielding effect simplify the inductor modeling. A simple RLC network with a frequency dependent resistor can be closely matched to the inductor characteristic upto 20GHz.

Several vertical solenoid inductors were fabricated using standard 6-metal layer bulk CMOS process. Among different size inductors fabricated, the SRF of the smallest inductor of 1.74nH is 25.5GHz, while the largest inductor of 7.86nH is only 7.58GHz. By using 10-metal layer process, additional 56% increase in SRF and 63% reduction in area are expected for the 4.8nH inductor.

## II. Vertical Solenoid V.S. Planar Spiral

Two pairs of vertical solenoid and planar spiral inductors of similar inductance were fabricated in the same chip for comparison. Either poly PGS or NWELL were put underneath the inductors to investigate their impacts on inductor quality-factor and self-resonant frequency. The die photos of the solenoid and spiral inductors with poly PGS underneath were shown in Fig. 1.

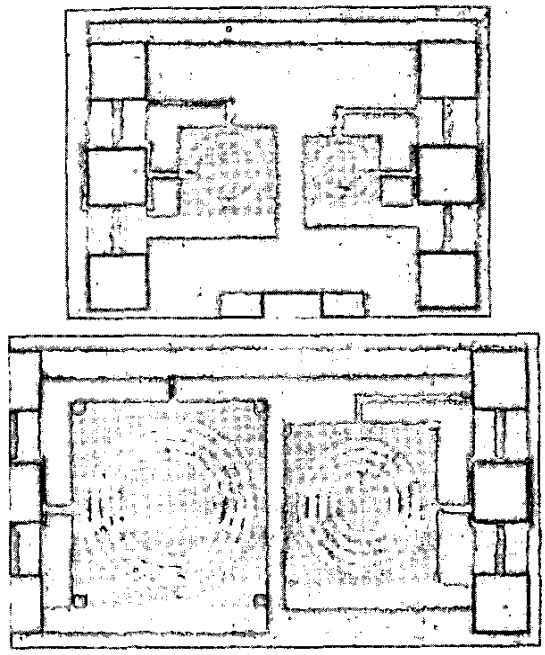

Fig. 1 Die photos of vertical solenoid inductors (top, 4.8nH and 2.8nH) and planar spiral inductors (bottom, 4.1nH and 2.4nH). Poly patterned-ground-shield is used underneath the inductor.

One advantage of the solenoid structure is that the whole inductor is self-shielded electrically from the lossy substrate by the bottom coil as illustrated by the cross-section view of the inductors in Fig. 2. Using poly PGS has insignificant improvement on QF in contrast to the case of spiral inductor as shown in Fig. 3. Furthermore, the poly PGS reduces the SRF of inductor which is undesirable.

It has been shown in [3] that inner inductor coils contribute little inductance but large resistance due to eddie current induced by the magnetic field of the inductor. Hollow inductor is recommended with few turns used. It is also recommended that the inductor size should be kept small so that the magnetic field would not penetrate deep into the lossy substrate which will reduce the inductance and QF. So, a trade-off is needed for optimal combination. Unless a



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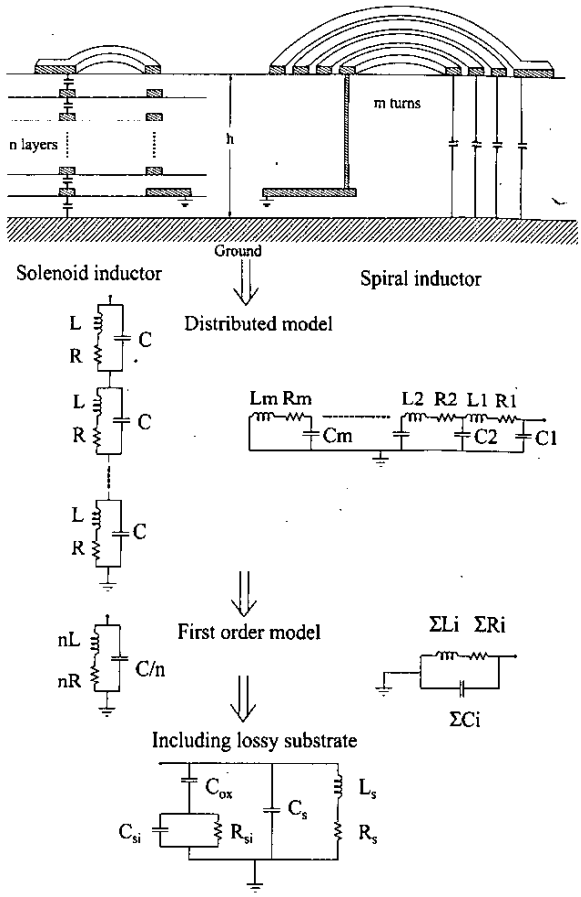


Fig. 2 Simple lump model for solenoid and spiral inductors. The parasitic capacitance of the solenoid inductor is dominated by inter-metal capacitance Cs = C/n. The parasitic capacitance of the spiral inductor is dominated by metal to substrate capacitance Cox = ΣCi. For same inductance, the solenoid inductor has smaller total parasitic capacitance than spiral inductor and hence higher self-resonant frequency.

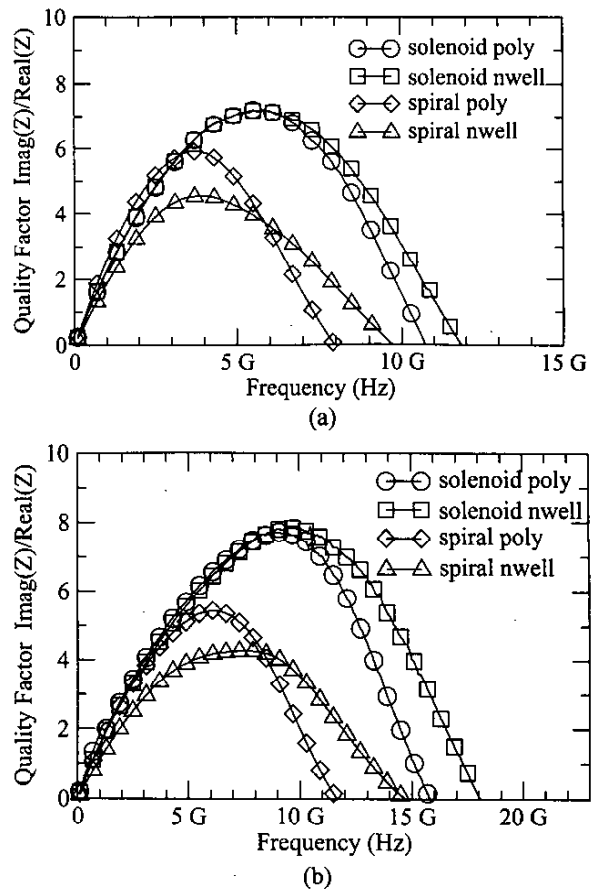


Fig. 3 The quality factors of (a) 4.8nH solenoid and 4.1nH spiral inductors, (b) 2.8nH solenoid and 2.4nH spiral inductors. The SRF is the frequency where quality factor equals zero. The poly PGS improves the maximum quality factor for the spiral inductors but not for the solenoid inductors due to their self-shielding property. Poly PGS reduces the SRF for both inductors.

one turn inductor is used, which is rare [4] and area inefficient, inner turns always suffer from higher eddie current loss. Using solenoid structure, there is only one turn in every metal layer and the size is much smaller than the spiral type.

Although solenoid inductor has larger metal to metal overlapping capacitance, the SRF of the larger inductance solenoid inductor is still much higher than that of the planar spiral inductor as shown in the zero-crossing frequency of the QF in Fig. 3. It is because each metal to metal capacitor only resonates with a small inductor as shown in the distributed model in Fig. 2. The effective inter-metal capacitance Cs of the solenoid inductor is equivalent to the capacitance of a single coil at the height of h/2, assuming that the metal thickness and the inter-metal dielectric thickness are the same. Together with smaller area covered by the inductor wire, the parasitic capacitance of the solenoid inductor is much smaller than that of the same inductance spiral inductor.

Although the distance between the top metal layer and the substrate (h) is increasing with newer technology due to the increased number of metal layers, the percentage of increase in h and SRF of the planar spiral inductor as technology grows levels off. On the other hand, the vertical solenoid inductor will continuously be benefited from the newer technology as more turn reduces the inductor area. Fig. 4 shows the solenoid inductor's QF with different number of metal layers using EM simulation.

In the case that the inductor is used in a resonator with a tuning capacitor, the QF ($Q_\phi$) derived from the rate of

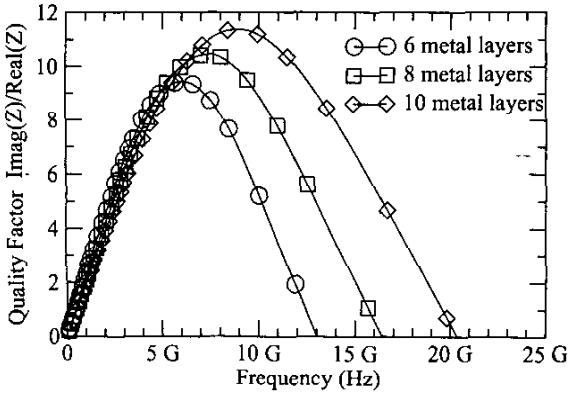


Fig. 4 Simulated quality factor of 4.8nH solenoid inductors with different number of metal layers using EM simulation. For metal layers increased from 6 to 10, the self-resonant frequency is increased by 56% while the inductor area is reduced by 63% (external radius is reduced from 54μm to 33μm). The maximum quality factor is also increased by 20%.

phase change at resonant is more appropriate for comparison[5]. By adding an ideal capacitor parallel to the inductor, we can derive that

$$Q_\phi = \frac{1}{2}\left|\frac{f}{Y_R}\frac{dY_I}{df} - \frac{Y_I}{Y_R}\right| \qquad (1)$$

where $Y_R$ and $Y_I$ are the real and imaginary part of the inductor admittance respectively. Physically, the rate of admittance change of a inductor and a capacitor have opposite sign. We can subtract the admittance due to the capacitor using the product of frequency and first derivative of the imaginary admittance. The $Q_\phi$ of the spirals compared with other solenoids with similar inductance are shown in Fig. 5. Solenoid inductors offer superior as frequency increases.

## III. Inductor Modeling

The self-shielding property of the vertical solenoid inductor simplifies the inductor modeling by ignoring the substrate resistance Rsi. The solenoid inductor can be modeled by a constant capacitor Cs in parallel to the series inductor Ls and resistor Rs. Fig. 6 shows the extracted inductance Ls for both solenoid inductor and spiral inductor. The Ls of the solenoid inductor is roughly constant while the Ls of the spiral inductor rolls off significantly indicating that the finite poly PGS resistance Rsi cannot be ignored for the planar spiral inductor. There is about 0.2nH inductance reduction for Ls at low frequency. This is due to the skin effect which decreases the internal inductance. Constant inductor Ls can be used to model the inductor for

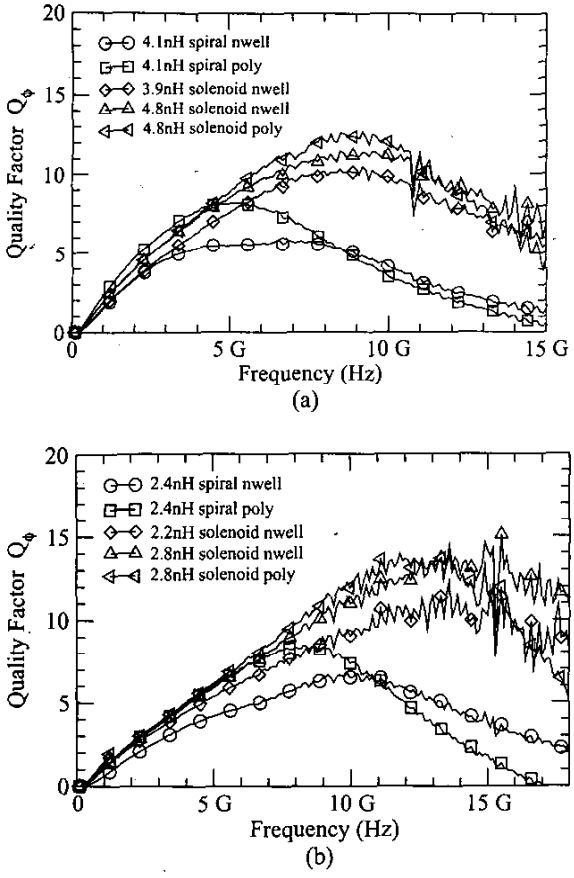


Fig. 5 The quality factor of the inductor derived from the rate of phase change at resonant, tuned by an ideal capacitor. Solenoid inductors have higher quality factor and poly PGS provides only little improvement.

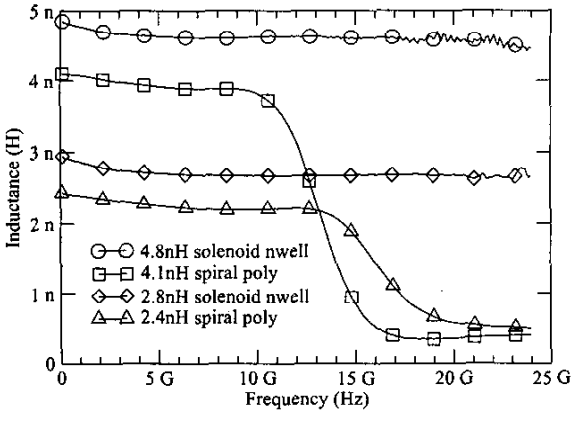


Fig. 6 Extracted inductance Ls when Cs is constant.

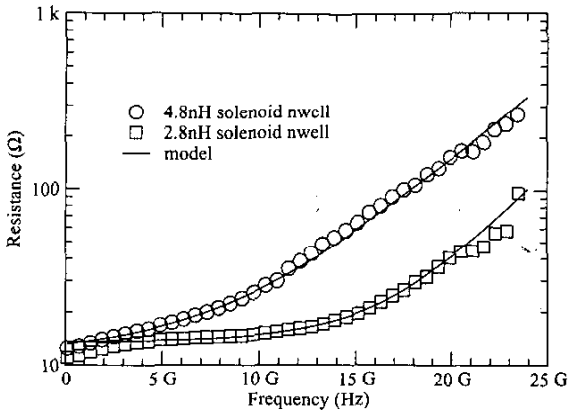


Fig. 7 Extracted Rs when Cs is constant.

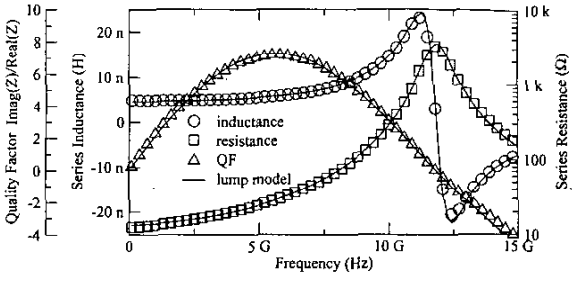


Fig. 8 The impedance and QF of the 4.8nH solenoid inductor. The simple RLC circuit can closely matched to the measurement data.

high frequency applications. Fig. 7 shows the extracted Rs for the solenoid inductor. Equation $R_s = a + 10^{b(f+c)}$ is used to model the frequency dependant nature of the resistor which is also due to the skin effect. Variable a, b and c are fitting parameters while f is the frequency. Using simple inductor model consisting a constant capacitor, a constant inductor and a frequency dependant resistor, we can accurately describe the solenoid inductor behavior as shown in Fig. 8.

## IV. Conclusion

A vertical solenoid inductor structure was proposed for on-chip inductor in CMOS process. Experiment results show that higher quality-factor and self-resonant frequency can be obtained compared to the planar spiral inductor. The compact design also reduces the cost by saving chip area. The inductor can be modeled by a simple RLC circuit over wide frequency range.The performance of solenoid inductors is summarized in Fig. 9. The frequency for maximum QF is different for different QF definition. Using which definition for design optimization is application dependent. The largest inductor of 7.86nH is still usable for 5GHz application.

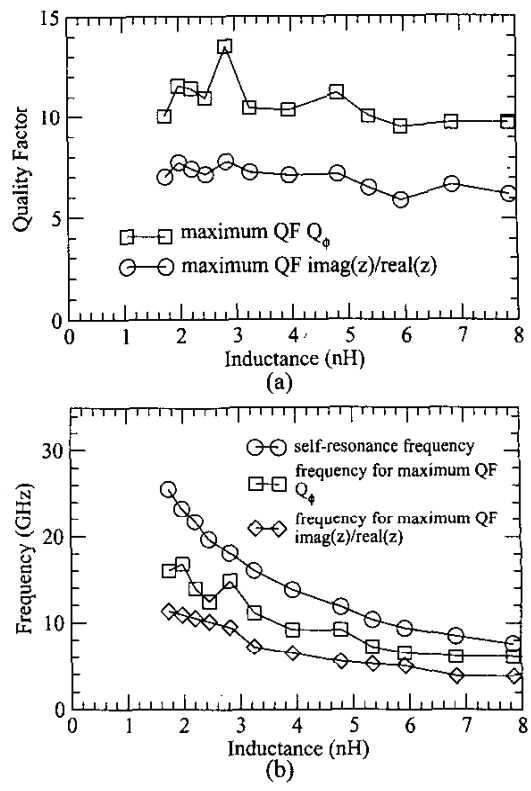


Fig. 9 Several solenoid inductors of different size with nwell were measured. (a) The maximum quality factors, (b) the self-resonant frequency and the frequency where quality factors are maximum.


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